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Stability of the 7-3 Compressor Circuit for Wallace Tree. Part I[1]

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Summary. To evaluate our formal verification method on a real-size calculation circuit, in this article, we continue to formalize the concept of the 7-3 Compressor (STC) Circuit [6] for Wallace Tree [11], to define the structures of calculation units for a very fast multiplication algorithm for VLSI implementation [10]. We define the circuit structure of the tree constructions of the Generalized Full Adder Circuits (GFAs). We then successfully prove its circuit stability of the calculation outputs after four and six steps. The motivation for this research is to establish a technique based on formalized mathematics and its applications for calculation circuits with high reliability, and to implement the applications of the reliable logic synthesizer and hardware compiler [5].

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Keywords: arithmetic processor; high order compressor; high-speed multiplier; Wallace tree; logic circuit stability

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0. Introduction

Since calculation models of the arithmetic logic unit based on many sorted algebra have been proposed, we continue to verify the structure and design of these circuits using the Mizar [2], [3], [4] proof checking system. Actually, the stability of circuit primitives is proved based on the definitions and theorems on logic operations, hardware gates, and signal lines [8], [9], [7].

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The various concepts for the Boolean operations, the logic gate elements needed to define the digital circuit, and the connections are defined and have been proved [1]. For logic gate elements that compose a calculation circuit using many Boolean operations, we have prepared a practical collection of logic gates [13]. To construct the adder circuit structure for the RSD numeric representation, we then formalized the definitions and properties of the Generalized Full Adder Circuits (GFAs) to have three inputs and two outputs [14]. Since we have to scale the size of evaluation up to this formal verification method on a real-size calculation circuit, we have already completed formalize the concept of the 4-2 Binary Addition Cell primitives (FTAs) [12] to construct the structures of calculation units for a very fast multiplication algorithm for VLSI implementation [10].

There is the Wallace tree multiplication method [11] as achieved high-speed multiplier, which is connected like the tree using the usual full adder (FA) circuit cell. Since it transforms the Wallace tree multiplication method to improve the high-speed computation and circuit regularity, there is also a refinement multiplication method using the 7-3 Compressor Circuit [6].

We show the component symbol and the block diagram of a 7-3 Compressor Circuit implementation in Figure 1 and Figure 2 using four GFAs. First two GFAs take six of the seven inputs (x1,x2,x3,x5,x6,x7) and generate two sum (A1,A2) and two carry outputs (C1,C2) in Layer-I (after 2-steps). The sum outputs are combined with the seventh input (x4) in another GFA to generate the s0 output of the 7-3 Compressor in Layer-II (after 4-steps). The carry output of this GFA is combined with the carry outputs from the two first level GFAs using fourth GFA to yield s1 and s2, with weights of two and four respectively in Layer-III (after 6-steps).

```
   x1 x2 x3 x4 x5 x6 x7     Inputs  : x1,x2,...,x7 (without pair)
   |  |  |  |  |  |  |
 +-*--*--*--*--*--*--*-+
 |                     |
 |      STC TYPE-0     |
 |                     |
 +------*---*---*------+
        |   |   |
       s2  s1  s0           Outputs : s2,s1,s0 (pair)

Composition : Cascading tree together with four GFA TYPE-0
Function    : [s2:s1:s0] = bit_count_of_<x1,x2,...,x7>
```

Fig.1 7-3 Compressor Circuit (Seven-to-Three Compressor:STC): TYPE-0, Component Symbol.

```
         7-inputs      x1   x2  x3  x4   x5   x6  x7    ..............
                       |    /   /   /    |    /   /
                   +---*---*   /   / +---*---*   /
                   |  GFA  *__/   /  |  GFA  *__/
                   | TYPE0 |     /   | TYPE0 |         LAYER-I
                   *---*---+    /    *---*---+         (2-steps)
                  /    |       /    /   /                      |
           C1 ___/   A1|      /  C2/ A2/      .................V......
             /    _____|_____/____/   /
            /    /     |    /        /
           /    /  +---*---*        /
          /    /   |  GFA  *_______/                   LAYER-II
         /    /    | TYPE0 |                           (4-steps)
        /    /     *---*---+                                   |
     C1|  C2/   C3/ A3/                 .......................V......
   +---*---*     /   /
   |  GFA  *____/   /
   | TYPE0 |   ____/                                   LAYER-III
   *---*---+  /                                        (6-steps)
  /    |     /                                                 |
 s2   s1    s0     3-outputs     ..............................V......

Intermediate Outputs (2-steps):
  C1 := GFA0CarryOutput(x1,x2,x3)
  C2 := GFA0CarryOutput(x5,x6,x7)
  A1 := GFA0AdderOutput(x1,x2,x3)
  A2 := GFA0AdderOutput(x5,x6,x7)
Intermediate Output (4-steps):
  C3 := GFA0CarryOutput(A1,A2,x4)
External Outputs    (4,6-steps):
  s0 := GFA0AdderOutput(A1,A2,x4) (=A3)
  s1 := GFA0AdderOutput(C1,C2,C3)
  s2 := GFA0CarryOutput(C1,C2,C3)

Composite Circuit Structure:
  ( ( BitGFA0Str(x1,x2,x3) ++ BitGFA0Str(x5,x6,x7) )  # STC0IIStr
   ++ BitGFA0Str(A1,A2,x4) )                          # STC0IStr
   ++ BitGFA0Str(C1,C2,C3)                            # STC0Str
   --->
      STC0Str(x1,x2,x3,x4,x5,x6,x7)
```

Fig.2 7-3 Compressor Circuit, Block Diagram and Calculation Stability: Following(s,6) is stable.

1. Properties of 'Intermediate' STC Circuit Structure (LAYER-I)

Let x_1, x_2, x_3, x_4 be non pair objects. Let us note that $\{x_1, x_2, x_3, x_4\}$ has no pairs.

Let x_5 be a non pair object. Observe that $\{x_1, x_2, x_3, x_4, x_5\}$ has no pairs.

Let x_6 be a non pair object. Let us note that $\{x_1, x_2, x_3, x_4, x_5, x_6\}$ has no pairs.

Let x_7 be a non pair object. One can verify that $\{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$ has no pairs.

Let x_1, x_2, x_3, x_5, x_6, x_7 be sets. The functor STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$ yielding an unsplit, non void, strict, non empty many sorted signature with arity held in gates and Boolean denotation held in gates is defined by the term

(Def. 1) BitGFA0Str(x_1, x_2, x_3)+· BitGFA0Str(x_5, x_6, x_7).

The functor STC0IICirc$(x_1, x_2, x_3, x_5, x_6, x_7)$ yielding a strict, Boolean circuit of STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$ with denotation held in gates is defined by the term

(Def. 2) BitGFA0Circ(x_1, x_2, x_3)+· BitGFA0Circ(x_5, x_6, x_7).

Let us consider sets x_1, x_2, x_3, x_5, x_6, x_7. Now we state the propositions:

(1) InnerVertices(STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$) $=$ $((\{\langle\langle x_1, x_2\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_1, x_2, x_3)\} \cup \{\langle\langle x_1, x_2\rangle, \mathrm{and}_2\rangle, \langle\langle x_2, x_3\rangle, \mathrm{and}_2\rangle, \langle\langle x_3, x_1\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_1, x_2, x_3)\}) \cup \{\langle\langle x_5, x_6\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_5, x_6, x_7)\}) \cup \{\langle\langle x_5, x_6\rangle, \mathrm{and}_2\rangle, \langle\langle x_6, x_7\rangle, \mathrm{and}_2\rangle, \langle\langle x_7, x_5\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_5, x_6, x_7)\}$.

(2) InnerVertices(STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$) is a binary relation.

Let us consider non pair sets x_1, x_2, x_3, x_5, x_6, x_7. Now we state the propositions:

(3) InputVertices(STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$) $= \{x_1, x_2, x_3, x_5, x_6, x_7\}$.

(4) InputVertices(STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$) has no pairs.

Let us consider sets x_1, x_2, x_3, x_5, x_6, x_7. Now we state the propositions:

(5) x_1, x_2, x_3, x_5, x_6, x_7, $\langle\langle x_1, x_2\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_1, x_2, x_3)$, $\langle\langle x_1, x_2\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_2, x_3\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_3, x_1\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_1, x_2, x_3)$, $\langle\langle x_5, x_6\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_5, x_6, x_7)$, $\langle\langle x_5, x_6\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_6, x_7\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_7, x_5\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_5, x_6, x_7)$ $\in$ the carrier of STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$.

(6) $\langle\langle x_1, x_2\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_1, x_2, x_3)$, $\langle\langle x_1, x_2\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_2, x_3\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_3, x_1\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_1, x_2, x_3)$, $\langle\langle x_5, x_6\rangle, \mathrm{xor}_2\rangle$,

GFA0AdderOutput(x_5, x_6, x_7), $\langle\langle x_5, x_6\rangle$, and$_2\rangle$, $\langle\langle x_6, x_7\rangle$, and$_2\rangle$, $\langle\langle x_7, x_5\rangle$, and$_2\rangle$, GFA0CarryOutput($x_5, x_6, x_7$) $\in$ InnerVertices(STC0IIStr($x_1, x_2, x_3, x_5, x_6, x_7$)). The theorem is a consequence of (1).

(7) Let us consider non pair sets x_1, x_2, x_3, x_5, x_6, x_7. Then x_1, x_2, x_3, x_5, x_6, $x_7 \in$ InputVertices(STC0IIStr($x_1, x_2, x_3, x_5, x_6, x_7$)). The theorem is a consequence of (3).

Let $x_1, x_2, x_3, x_5, x_6, x_7$ be sets. The functors: STC0IICarryOutC1($x_1, x_2, x_3, x_5, x_6, x_7$), STC0IIAdderOutA1($x_1, x_2, x_3, x_5, x_6, x_7$), STC0IICarryOutC2($x_1, x_2, x_3, x_5, x_6, x_7$), and STC0IIAdderOutA2($x_1, x_2, x_3, x_5, x_6, x_7$) yielding elements of InnerVertices(STC0IIStr($x_1, x_2, x_3, x_5, x_6, x_7$)) are defined by terms

(Def. 3) GFA0CarryOutput(x_1, x_2, x_3),

(Def. 4) GFA0AdderOutput(x_1, x_2, x_3),

(Def. 5) GFA0CarryOutput(x_5, x_6, x_7),

(Def. 6) GFA0AdderOutput(x_5, x_6, x_7),

respectively. Now we state the propositions:

(8) Let us consider non pair sets x_1, x_2, x_3, x_5, x_6, x_7, a state s of STC0IICirc ($x_1, x_2, x_3, x_5, x_6, x_7$), and elements a_1, a_2, a_3, a_5, a_6, a_7 of *Boolean*. Suppose $a_1 = s(x_1)$ and $a_2 = s(x_2)$ and $a_3 = s(x_3)$ and $a_5 = s(x_5)$ and $a_6 = s(x_6)$ and $a_7 = s(x_7)$. Then

(i) (Following(s, 2))(STC0IICarryOutC1($x_1, x_2, x_3, x_5, x_6, x_7$)) $= (a_1 \wedge a_2 \vee a_2 \wedge a_3) \vee a_3 \wedge a_1$, and

(ii) (Following(s, 2))(STC0IIAdderOutA1($x_1, x_2, x_3, x_5, x_6, x_7$)) $= (a_1 \oplus a_2) \oplus a_3$, and

(iii) (Following(s, 2))(STC0IICarryOutC2($x_1, x_2, x_3, x_5, x_6, x_7$)) $= (a_5 \wedge a_6 \vee a_6 \wedge a_7) \vee a_7 \wedge a_5$, and

(iv) (Following(s, 2))(STC0IIAdderOutA2($x_1, x_2, x_3, x_5, x_6, x_7$)) $= (a_5 \oplus a_6) \oplus a_7$, and

(v) (Following(s, 2))(x_1) $= a_1$, and

(vi) (Following(s, 2))(x_2) $= a_2$, and

(vii) (Following(s, 2))(x_3) $= a_3$, and

(viii) (Following(s, 2))(x_5) $= a_5$, and

(ix) (Following(s, 2))(x_6) $= a_6$, and

(x) (Following(s, 2))(x_7) $= a_7$.

The theorem is a consequence of (7).

(9) Let us consider non pair sets x_1, x_2, x_3, x_5, x_6, x_7, and a state s of STC0IICirc($x_1, x_2, x_3, x_5, x_6, x_7$). Then Following($s$, 2) is stable.

2. Properties of 'Intermediate' STC Circuit Structure (LAYER-II)

Let x_1, x_2, x_3, x_4, x_5, x_6, x_7 be sets. The functor STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$ yielding an unsplit, non void, strict, non empty many sorted signature with arity held in gates and Boolean denotation held in gates is defined by the term

(Def. 7) STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$+· BitGFA0Str(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4)$.

The functor STC0ICirc$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$ yielding a strict, Boolean circuit of STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$ with denotation held in gates is defined by the term

(Def. 8) STC0IICirc$(x_1, x_2, x_3, x_5, x_6, x_7)$+· BitGFA0Circ(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4)$.

Let us consider sets x_1, x_2, x_3, x_4, x_5, x_6, x_7.

Now we state the propositions:

(10) InnerVertices(STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) = $\{\langle\langle x_1, x_2\rangle$, xor$_2\rangle$, GFA0AdderOutput$(x_1, x_2, x_3)\}\cup$ $\{\langle\langle x_1, x_2\rangle$, and$_2\rangle$, $\langle\langle x_2, x_3\rangle$, and$_2\rangle$, $\langle\langle x_3, x_1\rangle$, and$_2\rangle$, GFA0CarryOutput$(x_1, x_2, x_3)\}\cup$ $\{\langle\langle x_5, x_6\rangle$, xor$_2\rangle$, GFA0AdderOutput$(x_5, x_6, x_7)\}\cup$ $\{\langle\langle x_5, x_6\rangle$, and$_2\rangle$, $\langle\langle x_6, x_7\rangle$, and$_2\rangle$, $\langle\langle x_7, x_5\rangle$, and$_2\rangle$, GFA0CarryOutput$(x_5, x_6, x_7)\}\cup$ $\{\langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, xor$_2\rangle$, GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput $(x_5, x_6, x_7), x_4)\}\cup$ $\{\langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, and$_2\rangle$, $\langle\langle$GFA0AdderOutput$(x_5, x_6, x_7), x_4\rangle$, and$_2\rangle$, $\langle\langle x_4$, GFA0AdderOutput $(x_1, x_2, x_3)\rangle$, and$_2\rangle$, GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4)\}$.

The theorem is a consequence of (1).

(11) InnerVertices(STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) is a binary relation.

(12) Let us consider non pair sets x_1, x_2, x_3, x_5, x_6, x_7, and a set x_4. Suppose $x_4 \neq \langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, xor$_2\rangle$ and $x_4 \neq \langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, and$_2\rangle$ and $x_4 \notin$ InnerVertices(STC0IIStr$(x_1, x_2, x_3, x_5, x_6, x_7)$). Then InputVertices(STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) = $\{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$. The theorem is a consequence of (1) and (3).

Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7.

(13) InputVertices(STC0IStr($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) $= \{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$. The theorem is a consequence of (12).

(14) InputVertices(STC0IStr($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) has no pairs. The theorem is a consequence of (13).

Let us consider sets x_1, x_2, x_3, x_4, x_5, x_6, x_7.

(15) $x_1, x_2, x_3, x_4, x_5, x_6, x_7$, $\langle\langle x_1, x_2\rangle$, xor$_2\rangle$, GFA0AdderOutput($x_1, x_2, x_3$), $\langle\langle x_1, x_2\rangle$, and$_2\rangle$, $\langle\langle x_2, x_3\rangle$, and$_2\rangle$, $\langle\langle x_3, x_1\rangle$, and$_2\rangle$, GFA0CarryOutput($x_1$, x_2, x_3), $\langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7)$\rangle$, xor$_2\rangle$, GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0Adder Output(x_5, x_6, x_7), x_4), $\langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOut− put(x_5, x_6, x_7)$\rangle$, and$_2\rangle$, $\langle\langle$GFA0AdderOutput(x_5, x_6, x_7), $x_4\rangle$, and$_2\rangle$, $\langle\langle x_4$, GFA0AdderOutput(x_1, x_2, x_3)$\rangle$, and$_2\rangle$ $\in$ the carrier of STC0IStr(x_1, x_2, x_3, x_4, x_5, x_6, x_7).

And also GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0 AdderOutput(x_5, x_6, x_7), x_4), $\langle\langle x_5, x_6\rangle$, xor$_2\rangle$, GFA0AdderOutput($x_5, x_6$, x_7), $\langle\langle x_5, x_6\rangle$, and$_2\rangle$, $\langle\langle x_6, x_7\rangle$, and$_2\rangle$, $\langle\langle x_7, x_5\rangle$, and$_2\rangle$, GFA0CarryOut− put($x_5, x_6, x_7$) $\in$ the carrier of STC0IStr($x_1, x_2, x_3, x_4, x_5, x_6, x_7$). The theorem is a consequence of (5).

(16) $\langle\langle x_1, x_2\rangle$, xor$_2\rangle$, GFA0AdderOutput($x_1, x_2, x_3$), $\langle\langle x_1, x_2\rangle$, and$_2\rangle$, $\langle\langle x_2$, $x_3\rangle$, and$_2\rangle$, $\langle\langle x_3, x_1\rangle$, and$_2\rangle$, GFA0CarryOutput($x_1, x_2, x_3$), $\langle\langle$GFA0Adder Output(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7)$\rangle$, xor$_2\rangle$, GFA0Adder Output(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7), x_4), $\langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7)$\rangle$, and$_2\rangle$, $\langle\langle$GFA0AdderOutput(x_5, x_6, x_7), $x_4\rangle$, and$_2\rangle$, $\langle\langle x_4$, GFA0AdderOutput (x_1, x_2, x_3)$\rangle$, and$_2\rangle$, GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7), x_4), $\langle\langle x_5, x_6\rangle$, xor$_2\rangle$, GFA0AdderOutput ($x_5, x_6, x_7$), $\langle\langle x_5, x_6\rangle$, and$_2\rangle$, $\langle\langle x_6, x_7\rangle$, and$_2\rangle$, $\langle\langle x_7, x_5\rangle$, and$_2\rangle$, GFA0Carry Output($x_5, x_6, x_7$) $\in$ InnerVertices(STC0IStr($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)). The theorem is a consequence of (10).

(17) Let us consider non pair sets x_1, x_2, x_3, x_5, x_6, x_7, and a set x_4. Suppose $x_4 \neq \langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7)$\rangle$, xor$_2\rangle$ and $x_4 \neq \langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7)$\rangle$, and$_2\rangle$ and $x_4 \notin$ InnerVertices(STC0IIStr($x_1, x_2, x_3, x_5, x_6, x_7$)). Then x_1, x_2, x_3, x_4, x_5, x_6, $x_7 \in$ InputVertices(STC0IStr(x_1, x_2, x_3, x_4, x_5, x_6, x_7)). The theorem is a consequence of (12).

(18) Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7. Then x_1, x_2, x_3, x_4, x_5, x_6, $x_7 \in$ InputVertices(STC0IStr($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)). The theorem is a consequence of (13).

Let $x_1, x_2, x_3, x_4, x_5, x_6, x_7$ be sets. The functors: STC0ICarryOutC1($x_1, x_2, x_3, x_4, x_5, x_6, x_7$), STC0ICarryOutC2($x_1, x_2, x_3, x_4, x_5, x_6, x_7$), STC0ICarry OutC3($x_1, x_2, x_3, x_4, x_5, x_6, x_7$), and STC0IAdderOutA3($x_1, x_2, x_3, x_4, x_5, x_6, x_7$) yielding elements of InnerVertices(STC0IStr($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) are defined by terms

(Def. 9) GFA0CarryOutput(x_1, x_2, x_3),

(Def. 10) GFA0CarryOutput(x_5, x_6, x_7),

(Def. 11) GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput (x_5, x_6, x_7), x_4),

(Def. 12) GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput (x_5, x_6, x_7), x_4),

respectively.

Now we state the propositions:

(19) Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7, a state s of STC0ICirc($x_1, x_2, x_3, x_4, x_5, x_6, x_7$), and elements a_1, a_2, a_3, a_4, a_5, a_6, a_7 of *Boolean*. Suppose $a_1 = s(x_1)$ and $a_2 = s(x_2)$ and $a_3 = s(x_3)$ and $a_4 = s(x_4)$ and $a_5 = s(x_5)$ and $a_6 = s(x_6)$ and $a_7 = s(x_7)$. Then

- (i) (Following($s, 2$))(STC0ICarryOutC1($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) $= (a_1 \wedge a_2 \vee a_2 \wedge a_3) \vee a_3 \wedge a_1$, and
- (ii) (Following($s, 2$))(STC0ICarryOutC2($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) $= (a_5 \wedge a_6 \vee a_6 \wedge a_7) \vee a_7 \wedge a_5$, and
- (iii) (Following($s, 4$))(STC0ICarryOutC3($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) $= (((a_1 \oplus a_2) \oplus a_3) \wedge ((a_5 \oplus a_6) \oplus a_7) \vee ((a_5 \oplus a_6) \oplus a_7) \wedge a_4) \vee a_4 \wedge ((a_1 \oplus a_2) \oplus a_3)$, and
- (iv) (Following($s, 4$))(STC0IAdderOutA3($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)) $= (((((a_1 \oplus a_2) \oplus a_3) \oplus a_4) \oplus a_5) \oplus a_6) \oplus a_7$, and
- (v) (Following($s, 4$))(x_1) $= a_1$, and
- (vi) (Following($s, 4$))(x_2) $= a_2$, and
- (vii) (Following($s, 4$))(x_3) $= a_3$, and
- (viii) (Following($s, 4$))(x_4) $= a_4$, and
- (ix) (Following($s, 4$))(x_5) $= a_5$, and
- (x) (Following($s, 4$))(x_6) $= a_6$, and
- (xi) (Following($s, 4$))(x_7) $= a_7$.

(20) Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7, and a state s of STC0ICirc($x_1, x_2, x_3, x_4, x_5, x_6, x_7$). Then Following($s, 4$) is stable. The theorem is a consequence of (9).

3. Properties of STC Circuit Structure (LAYER-III)

Let x_1, x_2, x_3, x_4, x_5, x_6, x_7 be sets. The functor STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$ yielding an unsplit, non void, strict, non empty many sorted signature with arity held in gates and Boolean denotation held in gates is defined by the term

(Def. 13) STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$+· BitGFA0Str(STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC3$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$).

The functor STC0Circ$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$ yielding a strict, Boolean circuit of STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$ with denotation held in gates is defined by the term

(Def. 14) STC0ICirc$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$+· BitGFA0Circ(STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC3$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$).

Let us consider sets x_1, x_2, x_3, x_4, x_5, x_6, x_7. Now we state the propositions:

(21) InnerVertices(STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) = InnerVertices(STC0IStr$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$)$\cup$ $\{\langle\langle$STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)\rangle$, $\mathrm{xor}_2\rangle$, GFA0AdderOutput(STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICa–rryOutC3$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$)$\}\cup$ $\{\langle\langle$STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC3$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$STC0ICarryOutC3$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, GFA0CarryOutput(STC0ICarryOutC1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, STC0ICarryOutC3$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$)$\}$.

(22) InnerVertices(STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) = $\{\langle\langle x_1, x_2\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_1, x_2, x_3)\} \cup \{\langle\langle x_1, x_2\rangle, \mathrm{and}_2\rangle, \langle\langle x_2, x_3\rangle, \mathrm{and}_2\rangle, \langle\langle x_3, x_1\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_1, x_2, x_3)\}\cup\{\langle\langle x_5, x_6\rangle, \mathrm{xor}_2\rangle$, GFA0AdderOutput$(x_5, x_6, x_7)\} \cup \{\langle\langle x_5, x_6\rangle, \mathrm{and}_2\rangle, \langle\langle x_6, x_7\rangle, \mathrm{and}_2\rangle, \langle\langle x_7, x_5\rangle, \mathrm{and}_2\rangle$, GFA0CarryOutput$(x_5, x_6, x_7)\} \cup \{\langle\langle$GFA0AdderOutput$(x_1, x_2, x_3)$, GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{xor}_2\rangle$, GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7), x_4)$\} \cup \{\langle\langle$GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$GFA0AdderOutput$(x_5, x_6, x_7), x_4\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle x_4$, GFA0AdderOutput$(x_1, x_2, x_3)\rangle$, $\mathrm{and}_2\rangle$, GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7),

$x_4)\} \cup \{\langle\langle$GFA0CarryOutput$(x_1, x_2, x_3)$, GFA0CarryOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{xor}_2\rangle$, GFA0AdderOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0Carry Output(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4))\} \cup \{\langle\langle$GFA0CarryOutput$(x_1, x_2, x_3)$, GFA0CarryOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$GFA0CarryOutput(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput $(x_5, x_6, x_7), x_4)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4)$, GFA0CarryOutput$(x_1, x_2, x_3)\rangle$, $\mathrm{and}_2\rangle$, GFA0CarryOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0Carry Output(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4))\}$. The theorem is a consequence of (21) and (10).

(23) InnerVertices(STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) is a binary relation.

Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7.

(24) InputVertices(STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)) = \{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$. The theorem is a consequence of (10), (14), and (13).

(25) InputVertices(STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) has no pairs. The theorem is a consequence of (24).

Let us consider sets x_1, x_2, x_3, x_4, x_5, x_6, x_7.

(26) x_1, x_2, x_3, x_4, x_5, x_6, x_7, $\langle\langle x_1, x_2\rangle, \mathrm{xor}_2\rangle$, $\langle\langle x_1, x_2\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_2, x_3\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_3, x_1\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_5, x_6\rangle, \mathrm{xor}_2\rangle$, $\langle\langle x_5, x_6\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_6, x_7\rangle, \mathrm{and}_2\rangle$, $\langle\langle x_7, x_5\rangle, \mathrm{and}_2\rangle$, GFA0AdderOutput$(x_1, x_2, x_3)$, GFA0CarryOutput$(x_1, x_2, x_3)$, GFA0AdderOutput$(x_5, x_6, x_7)$, GFA0CarryOutput$(x_5, x_6, x_7)$, $\langle\langle$GFA0 AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{xor}_2\rangle$, $\langle\langle$GFA0Ad derOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$GFA0Add erOutput$(x_5, x_6, x_7), x_4\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle x_4$, GFA0AdderOutput$(x_1, x_2, x_3)\rangle$, $\mathrm{and}_2\rangle$ $\in$ the carrier of STC0Str$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$.

And also GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0Add erOutput$(x_5, x_6, x_7), x_4)$, GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4)$, $\langle\langle$GFA0CarryOutput(x_1, x_2, x_3), GFA0 CarryOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{xor}_2\rangle$, GFA0AdderOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOut– put(x_1, x_2, x_3), GFA0AdderOuput$(x_5, x_6, x_7), x_4))$, $\langle\langle$GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput$(x_5, x_6, x_7)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$GFA0CarryOutput(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput $(x_5,x_6,x_7), x_4)\rangle$, $\mathrm{and}_2\rangle$, $\langle\langle$GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput$(x_5, x_6, x_7), x_4)$, GFA0CarryOutput$(x_1, x_2, x_3)\rangle$, $\mathrm{and}_2\rangle$, GFA0CarryOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOut put(x_5, x_6, x_7), x_4)) ∈ the carrier of STC0Str($x_1, x_2, x_3, x_4, x_5, x_6, x_7$). The theorem is a consequence of (15).

(27) ⟨⟨x_1, x_2⟩, xor_2⟩, ⟨⟨x_1, x_2⟩, and_2⟩, ⟨⟨x_2, x_3⟩, and_2⟩, ⟨⟨x_3, x_1⟩, and_2⟩, ⟨⟨x_5, x_6⟩, xor_2⟩, ⟨⟨x_5, x_6⟩, and_2⟩, ⟨⟨x_6, x_7⟩, and_2⟩, ⟨⟨x_7, x_5⟩, and_2⟩, GFA0AdderOutput(x_1, x_2, x_3), GFA0CarryOutput(x_1, x_2, x_3), GFA0AdderOutput (x_5, x_6, x_7), GFA0CarryOutput(x_5, x_6, x_7), ⟨⟨GFA0AdderOutput(x_1, x_2, x_3),GFA0AdderOutput(x_5,x_6, x_7)⟩,xor_2⟩, ⟨⟨GFA0AdderOutput(x_1,x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7)⟩, and_2⟩, ⟨⟨GFA0AdderOutput(x_5, x_6, x_7), x_4⟩, and_2⟩, ⟨⟨x_4, GFA0AdderOutput(x_1, x_2, x_3)⟩, and_2⟩, GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7), x_4) GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6,x_7),x_4), ⟨⟨GFA0CarryOutput(x_1,x_2, x_3), GFA0CarryOutput(x_5,x_6, x_7)⟩, xor_2⟩, GFA0AdderOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput(x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0 Adder Output(x_5, x_6, x_7), x_4)) ∈ InnerVertices(STC0Str(x_1, x_2, x_3, x_4, x_5, x_6, x_7)).

And also ⟨⟨GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput (x_5, x_6, x_7)⟩, and_2⟩, ⟨⟨GFA0CarryOutput(x_5, x_6, x_7), GFA0CarryOutput (GFA0AdderOutput(x_1,x_2, x_3),GFA0AdderOutput(x_5, x_6, x_7), x_4)⟩, and_2⟩, ⟨⟨GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput (x_5, x_6, x_7), x_4), GFA0CarryOutput(x_1, x_2, x_3)⟩, and_2⟩, GFA0CarryOutput (GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput(x_5, x_6, x_7), GFA0Carry Output(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput(x_5, x_6, x_7), x_4)) ∈ Inner Vertices(STC0Str($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)). The theorem is a consequence of (22).

(28) Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7. Then x_1, x_2, x_3, x_4, x_5, x_6, x_7 ∈ InputVertices(STC0Str($x_1, x_2, x_3, x_4, x_5, x_6, x_7$)). The theorem is a consequence of (24).

Let x_1, x_2, x_3, x_4, x_5, x_6, x_7 be sets. The functors: STC0OutS0(x_1, x_2, x_3, x_4, x_5, x_6, x_7), STC0OutS1($x_1, x_2, x_3, x_4, x_5, x_6, x_7$), and STC0OutS2($x_1, x_2, x_3$, x_4, x_5, x_6, x_7) yielding elements of InnerVertices(STC0Str($x_1, x_2, x_3, x_4, x_5, x_6$, x_7)) are defined by terms

(Def. 15) GFA0AdderOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0AdderOutput (x_5, x_6, x_7), x_4),

(Def. 16) GFA0AdderOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput (x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0Ad−derOutput(x_5, x_6, x_7), x_4)),

(Def. 17) GFA0CarryOutput(GFA0CarryOutput(x_1, x_2, x_3), GFA0CarryOutput (x_5, x_6, x_7), GFA0CarryOutput(GFA0AdderOutput(x_1, x_2, x_3), GFA0Ad−

derOutput$(x_5, x_6, x_7), x_4)$),

respectively. Now we state the propositions:

(29) Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7, a state s of STC0Circ$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$, and elements a_1, a_2, a_3, a_4, a_5, a_6, a_7 of *Boolean*. Suppose $a_1 = s(x_1)$ and $a_2 = s(x_2)$ and $a_3 = s(x_3)$ and $a_4 = s(x_4)$ and $a_5 = s(x_5)$ and $a_6 = s(x_6)$ and $a_7 = s(x_7)$. Then

(i) (Following$(s, 4)$)(STC0OutS0$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) $= (((((a_1 \oplus a_2) \oplus a_3) \oplus a_4) \oplus a_5) \oplus a_6) \oplus a_7$, and

(ii) (Following$(s, 6)$)(STC0OutS1$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) $= (((a_1 \wedge a_2 \vee a_2 \wedge a_3) \vee a_3 \wedge a_1) \oplus ((a_5 \wedge a_6 \vee a_6 \wedge a_7) \vee a_7 \wedge a_5)) \oplus ((((a_1 \oplus a_2) \oplus a_3) \wedge ((a_5 \oplus a_6) \oplus a_7) \vee ((a_5 \oplus a_6) \oplus a_7) \wedge a_4) \vee a_4 \wedge ((a_1 \oplus a_2) \oplus a_3))$, and

(iii) (Following$(s, 6)$)(STC0OutS2$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$) $= (((a_1 \wedge a_2 \vee a_2 \wedge a_3) \vee a_3 \wedge a_1) \wedge ((a_5 \wedge a_6 \vee a_6 \wedge a_7) \vee a_7 \wedge a_5) \vee ((a_5 \wedge a_6 \vee a_6 \wedge a_7) \vee a_7 \wedge a_5) \wedge ((((a_1 \oplus a_2) \oplus a_3) \wedge ((a_5 \oplus a_6) \oplus a_7) \vee ((a_5 \oplus a_6) \oplus a_7) \wedge a_4) \vee a_4 \wedge ((a_1 \oplus a_2) \oplus a_3))) \vee ((((a_1 \oplus a_2) \oplus a_3) \wedge ((a_5 \oplus a_6) \oplus a_7) \vee ((a_5 \oplus a_6) \oplus a_7) \wedge a_4) \vee a_4 \wedge ((a_1 \oplus a_2) \oplus a_3)) \wedge ((a_1 \wedge a_2 \vee a_2 \wedge a_3) \vee a_3 \wedge a_1)$, and

(iv) (Following$(s, 6)$)$(x_1) = a_1$, and

(v) (Following$(s, 6)$)$(x_2) = a_2$, and

(vi) (Following$(s, 6)$)$(x_3) = a_3$, and

(vii) (Following$(s, 6)$)$(x_4) = a_4$, and

(viii) (Following$(s, 6)$)$(x_5) = a_5$, and

(ix) (Following$(s, 6)$)$(x_6) = a_6$, and

(x) (Following$(s, 6)$)$(x_7) = a_7$.

(30) Let us consider non pair sets x_1, x_2, x_3, x_4, x_5, x_6, x_7, and a state s of STC0Circ$(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$. Then Following$(s, 6)$ is stable. The theorem is a consequence of (20).

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